X-949 PATENT

ABSTRACT

A softPAL implementation and mapping method are described. The implementation utilizes both LUTs and architecture-specific logic circuits to implement softPAL functions, and selects from several implementations in order to decrease delay in function implementation. The method describes techniques for estimating p-terms in a 2-bounded sub-graph, factoring methods, mapping strategies for LUTs and dedicated logic elements, and delay optimization of critical paths.